AMENDMENTS TO THE CLAIMS

This Listing of Claims will replace all prior versions and listings of claims in the Application.

Listing of Claims:

Claim 1 (Currently amended): A method of providing forward error correction (FEC) to a data frame, the method comprising the steps of:

packetizing the data frame into a plurality of frame packets;

selecting portions of packet data from each of the plurality of frame packets, said selected portions being less than an entirety of a corresponding frame packet;

simultaneously concatenating only the selected portions of packet data from each of the plurality of frame packets into a concatenated bit field;

generating a forward error correction code for the concatenated bit field ~~selected portions of packet data exclusive of corresponding remaining portions of each of the plurality of frame packets~~; and

transmitting separately a packet containing the forward error correction code and the plurality of frame packets, the packet containing the forward error correction code being identified with a user data identifier code.

Claim 2 (Previously presented): The method as recited in claim 1, wherein the transmission of the forward error correction code in the separate packet is MPEG-4 compliant.

Claim 3 (Previously presented): The method as recited in claim 1, further including the step of transmitting the plurality of frame packets temporally prior to the separate forward error correction code packet transmitting step.

Claim 4 (Previously presented): The method as recited in claim 1, wherein the forward error correction code generating step includes the step of generating the forward error correction code as a Bose-Chaudhuri-Hocquenghem (BCH) code.

Claim 5 (Previously presented): The method as recited in claim 1, wherein the forward error correction code generating step includes the step of generating the forward error correction code as a systematic code.

Claim 6 (Previously presented): The method as recited in claim 1, wherein the packetizing step includes the step of separating the packet data into at least portions respectively and separately containing motion vector data and Discrete Cosine Transform (DCT) data.

Claim 7 (Currently amended): The method as recited in claim 6, wherein the packet data selecting step includes the step of selecting as the selected portions of packet data only header data, the motion vector data and ~~and~~ one of either a subset of the Discrete Cosine Transform (DCT) data or none of the Discrete Cosine Transform data.

Claim 8 (Previously presented): The method as recited in claim 1, wherein the packet data selecting step includes the step of selecting as the selected portions of packet data only packet data located between a resync field and a motion marker.

Claim 9 (Previously presented): The method as recited in claim 1, further comprising the steps of:

setting a flag indicating that a fixed Video Object Plane (VOP) increment is to set a fixed interval between each of the plurality of frame packets; and

assigning a fixed increment value to the fixed Video Object Plane increment.

Claim 10 (Currently amended): The method as recited in claim 1, further comprising the step of transmitting in the separate forward error correction code packet a value indicating a quantity of bits within at least a first packet of the

plurality of frame packets for which the forward error correction code ~~are~~ is generated.

Claim 11 (Currently amended): An error correction generating circuit, comprising:

a processor coupled to a processor readable memory;

a first instruction sequence stored in the processor memory and operable to cause the processor to select portions of packet data from each of a plurality of frame packets of a corresponding packetized data frame, said selected portions being less than an entirety of a corresponding frame packet;

a second instruction sequence stored in the processor readable memory and operable to cause the processor to simultaneously concatenate only the selected portions of packet data into a concatenated bit field;

a ~~second~~ third instruction sequence stored in the processor readable memory and operable to cause the processor to generate forward error correction data for the concatenated bit field ~~selected portions of packet data exclusive of the remaining portions of each of the plurality of frame packets~~;

a ~~third~~ fourth instruction sequence stored in the processor readable memory and operable to cause the processor to store the forward error correction data in a packet separate from the plurality of frame packets; and

a ~~fourth~~ fifth instruction sequence stored in the processor readable memory and operable to cause the processor to identify the separate packet with a data identifier code.

Claim 12 (Cancelled).

Claim 13 (Currently amended): The error correction generation circuit as recited in claim 11, further comprising a ~~fifth~~ sixth instruction sequence stored in the processor readable memory and operable to cause the processor to set a flag indicating that a fixed Video Object Plane (VOP) increment is to set a fixed interval between each of the plurality of frame packets and to assign a fixed increment value thereto.

Claim 14 (Currently amended): The error correction generation circuit as recited in claim 11, further comprising a ~~fifth~~ sixth instruction sequence stored in the processor readable memory and operable to cause the processor to provide a Header Extension Code (HEC) in every packet in a first sequence of packets.

Claim 15 (Previously presented): The error correction generation circuit as recited in claim 11, wherein the error correction generation circuit is incorporated on an integrated circuit.

Claim 16 (Previously presented): The error correction generation circuit as recited in claim 11, wherein the separate packet is MPEG-4 compliant.

Claim 17 (Previously presented): The error correction generation circuit as recited in claim 11, wherein the forward error correction data is generated using a Bose-Chaudhuri-Hocquenghem (BCH) code.

Claim 18 (Previously presented): The error correction generation circuit as recited in claim 11, wherein the forward error correction data is generated using a systematic code.

Claim 19 (Previously presented): The error correction generation circuit as recited in claim 11, wherein the packet data is separated into at least portions respectively and separately containing motion vector data and Discrete Cosine Transform (DCT) data.

Claim 20 (Previously presented): The error correction generation circuit as recited in claim 19, wherein the selected portions of packet data includes only header data, the motion vector data and one of either a subset of the Discrete Cosine Transform (DCT) data or none of the Discrete Cosine Transform data.

Claim 21 (Previously presented): The error correction generation circuit as recited in claim 11, wherein the selected portions of packet data is only the packet data located between a resync field and a motion marker.

Claim 22 (Currently amended): An encoder circuit, comprising:

means for generating forward error correction data for a concatenated bit field formed simultaneously from only selected portions of packet data from each of a plurality of frame packets, where the selected portions are less than an entirety of the corresponding frame packet ~~exclusive of the remaining portions of packet data in each of the plurality of frame packets~~;

means for storing the forward error correction data in a packet separate from the plurality of frame packets; and

means for identifying the separate packet with an identifier code.

Claim 23 (Cancelled).

Claim 24 (Currently amended): The encoder as recited in claim 22, further comprising ~~a~~ means for transmitting in the separate packet at least a value indicating a quantity of bits within at least a first packet of the plurality of frame packets for which forward error correction data was generated.